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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,061	11/21/2001	Hideki Yasuoka	XA-9574	1044

181 7590 02/04/2003

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/989,061	Applicant(s) YASUOKA ET AL
	Examiner Jennifer M. Kennedy	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *8,22 and 28-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-7, 9-21, 23-27, 59, 60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3, 6*.
4) ☐ Interview Summary (PTO-413) Paper No(s) _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election of Claims 1-7, 9-21, 23-27, and 59-60 in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 8, 22, and 28-58 arewithdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

Specification

The disclosure is objected to because of the following informalities:

On page 16, line 9, after "separated" the word –from-- should be inserted.

On page 20, line 1, "born" should be changed to –boron--.

On page 30, line 4, "filed" should be changed to –field--

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-12 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "said first conductive film forming region" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "first conductive film forming region " in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "said first conductive film forming region" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "said first conductive film forming region" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "said first semiconductor regions" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "said second semiconductor regions" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-7, 10-16, 21, 24 -26, and 59-60 rejected under 35 U.S.C. 102(b) as being anticipated by Taguchi (U.S. Patent No. 5,489,545).

Taguchi discloses the method of manufacturing a semiconductor integrated circuit device having a plurality of first MISFETs in a first region and plurality of second MISFETs in a second region, comprising the steps of:

forming a first insulating film (13) between two adjacent regions of the first MISFET forming regions in said first region and the second MISFET forming regions in the second region,

forming a second insulating film (16) over a surface of the semiconductor substrate between the first insulating films in each of the first and second regions,

depositing a third insulating film (18) over the second insulating film,

forming a first conductive film (20) over the third insulating film in the second region

forming, after removal of the third and second insulting films form the first region, a fourth insulating film (24) over the surface of the semiconductor substrate in the first region, and

forming a second conductive film (28) over the fourth insulating film,

wherein the third insulating film remains over the first insulating film in the second region.

In re claims 2-4, 6-7, and 10-11, Taguchi also discloses wherein the first insulating film is an oxide film formed by thermal oxidation (see column 2, lines 43-50), wherein the third insulating film is formed by CVD (see column 2, lines 52-55), wherein the etching rate of the third insulating film is greater than that of the first insulating film (see column 3, lines 45-50 and Figure 6), wherein the first and second conductive films are each made of polysilicon, wherein the third insulating film over the first insulating film is formed so that end portions of the third insulating film is position in the first insulating film (see Figure 4), wherein the first insulating film is formed at both ends of the first conductive film forming region within the second region (see Figure 2; FOX regions (14) surround the first conductive layers (20)), forming first semiconductor region (12) in the semiconductor substrate below the first insulating film formed at both ends of the first conductive film formed at both ends of the first conductive film forming region, and forming second semiconductor regions (32) with the first semiconductor regions but outside of the first insulating film formed at both ends of the first conductive film forming region.

In re claim 12, Taguchi discloses the method wherein the impurity concentration of the first semiconductor regions (rightmost side of substrate) is lower than that of the second semiconductor regions (12) (see Figure 1).

In re claim 13, Taguchi also discloses the method wherein the removal of the third insulating film from the first region is done without removing the third insulating film

from over the first insulating film in the second region (see Figure 3), and removing the first conductive film from the first region and a portion of the first conductive film for the second region (see Figure 2).

In re claim 14-16 and 21, Taguchi also discloses wherein the first insulating layer is an oxide film formed by thermal oxidation (see column 2, lines 43-50), wherein the third insulating film is formed by CVD (see column 2, lines 52-55), wherein the etching rate of the third insulating film is greater than that of the first insulating film (see column 3, lines 45-50 and Figure 6), wherein the first and second conductive films are each made of polysilicon.

In re claim 24, Taguchi also discloses removing a portion of the second and third insulating films over the second semiconductor region in the second region, thereby forming a first opening (see Figure 6), and forming a first semiconductor region (32) in the first region and a second semiconductor region (leftmost 36) in the second region, introducing an impurity on the surface of the semiconductor substrate in order to form third semiconductor regions (34) having a conductivity type contrary to that of the first semiconductor regions on both sides of the gate electrode of the first region and a fourth semiconductor region (rightmost 36) having the same conductivity type as that of the second semiconductors regions below the first opening in the second region (see Figure 7).

Further, in re claims 25-26, Taguchi discloses the method wherein the third insulating film constituting the first opening portion has sidewalls above the first

insulating film (see Figure 6), and wherein a fixed voltage is applied to the fourth semiconductor region (see column 1, lines 18-37).

In re claim 59 and 60, Taguchi discloses the method of forming a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region comprising the steps of:

forming a first insulating film made of a thermally oxidized film (16) over a surface of the semiconductor substrate in the first and second regions

depositing a second insulating film (18) over the first insulating film in the first and second region,

forming a first conductive film (20) over the second insulating film in the second region,

exposing the surface of the semiconductor substrate in the first region while covering the second insulating film in the second region with the first conductive film (see Figure 4), and forming a third insulating film made of thermally oxidized film (24). and

forming a second conductive film (28) over the third insulting film in the first region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains Patentability shall not be negatived by the manner in which the invention was made

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 5, 9, 20, 23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi (U.S. Patent No. 5,489,545).

Taguchi discloses the method substantially as claimed and rejected above, but does not disclose the relative thickness and widths of the insulative layers. It would have been obvious matter of design choice to form the structure having the claimed ranges of insulative thickness and width since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. In re Daily, 93 USPQ 47 (CCPA 1966), the court held that changes in size and shape of parts of an invention in the absence of an unexpected result involves routine skill in the art. Additionally, In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct form the prior art device. The selection of the thickness and width of the insulating layers is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re

Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi (U.S. Patent No. 5,489,545) in view of Barile et al. (U.S. Patent No. 3,793,090).

Taguchi discloses the method as substantially claimed and rejected above, but does not disclose the method of performing a heat treatment on the third insulating film at a temperature of 1000 degrees or greater. Barile et al. discloses the method of performing a heat treatment on the top layer of a gate dielectric at a temperature of 1000 degrees or greater (see abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to heat treat the gate layer prior to formation of that gate in order to reduce the large threshold voltage shifts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (703) 308-6171. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmk
January 24, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800